

## Claims

What is claimed is:

1. A method for tracing on a processor comprising:  
    executing an executing control block on the processor to obtain data, wherein an interrupt on the processor is disabled prior to executing the execution control block and the interrupt is enabling after execution of the execution control block is completed;  
    storing the data in a first buffer, wherein the first buffer is set to active; and  
    setting the first buffer to inactive and setting a second buffer to active, wherein the interrupt on the processor is disabled prior to switching the first buffer to inactive and the interrupt is enabling after setting the second buffer to active.
2. The method of claim 1, further comprising:  
    triggering a probe in an instrumented program; and  
    determining the execution control block associated with the probe.
3. The method of claim 2, further comprising:  
    associating the probe with a probe identifier.
4. The method of claim, 3 wherein the determining the execution control block associated with the probe comprises querying a global array.
5. The method of claim 4, wherein the probe identifier is used to query the global array.
6. A method of claim 3, further comprising:  
    associating the execution control block to the probe identifier.
7. The method of claim 1, wherein the execution control block comprises:

a predicate defining criterion for executing the execution control block;  
a consumer state component defining information associated with a consumer; and  
an action defining the data to be obtained from the instrumented program at the  
probe.

8. The method of claim 5, wherein the execution control block is an element in a linked list.
9. The method of claim 6, wherein the execution control block further comprises:  
a pointer to a next execution control block.
10. The method of claim 7, wherein the first buffer and the second buffer are associated with the consumer.
11. The method of claim 7, wherein periodically switching the first buffer to inactive and setting the second buffer to active comprises:  
searching for the first buffer and the second buffer associated with the consumer  
using the consumer state component.
12. The method of claim 1, wherein setting the first buffer to inactive and setting the second buffer to active occurs at a preset interval.
13. A system for tracing on a processor, comprising:  
a first buffer, wherein the first buffer is set to active;  
a second buffer, wherein the second buffer is set to inactive;  
an execution control block associated with a probe configured to obtain data from  
the probe; and  
a tracing framework configured to store the data in the first buffer and configured  
to set the first buffer to inactive and the second buffer to active, wherein the  
tracing framework is configured to issue a cross-call prior to setting the first  
buffer to inactive and the second buffer to active.

14. The system of claim 13, further comprising:  
an instrumented program comprising the probe.
15. The system of claim 13, further comprising:  
a consumer associated with the first buffer and the second buffer.
16. The system of claim 13, wherein the cross-call comprises disabling an interrupt on the processor prior to setting the first buffer to inactive and enabling the interrupt after setting the second buffer to active.
17. The system of claim 13, wherein the tracing framework is configured to disable an interrupt prior to obtaining data from the probe and enable the interrupt after obtaining data from the probe.
18. The system of claim 13, wherein the execution control block comprises:  
a predicate defining criterion for executing the execution control block;  
a consumer state component defining information associated with a consumer; and  
an action defining the data to be obtained from the instrumented program at the probe.
19. The system of claim 18, wherein the tracing framework is configured to obtain the execution control block associated with the probe using the consumer state.
20. The system of claim 13, wherein the first buffer comprises a drop count.
21. A network system having a plurality of nodes, comprising:  
a processor;  
a first buffer associated with the processor, wherein the first buffer is set to active;  
a second buffer associated with the processor, wherein the second buffer is set to inactive;

- an execution control block associated with a probe configured to obtain data from the probe; and
- a tracing framework configured to store the data in the first buffer and configured to set the first buffer to inactive and the second buffer to active, wherein the tracing framework is configured to issue a cross-call prior to setting the first buffer to inactive and the second buffer to active;
- wherein the processor executes on any node of the plurality of nodes,
- wherein the first buffer executes on any of the plurality of nodes,
- wherein the second buffer executes on any of the plurality of nodes,
- wherein the execution control block executes on any of the plurality of nodes, and
- wherein the tracing framework executes on any of the plurality of nodes.
22. The network of claim 21, wherein the cross-call comprises disabling an interrupt on the processor prior to setting the first buffer to inactive and enabling the interrupt after setting the second buffer to active.
23. The network of claim 21, wherein the execution control block comprises:
- a predicate defining criterion for executing the execution control block;
  - a consumer state component defining information associated with a consumer; and
  - an action defining the data to be obtained from the instrumented program at the probe.